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## TELECOPY/FACSIMILE

| To: | Company: | Fax Number: | Tel Number: |
|---|---|---|---|
| **Examiner: Vincent Lai**<br>**Art Unit: 2181** | **USPTO**<br>**Attn: Office of Petitions** | **571 – 273 - 8300** | |

From: Dariush G. Adli

Date: December 8, 2006

Time:

Total number of pages incl. cover page: 27

**For internal purposes only: Return to Diane Zynn**

Client number: **81751.0062**

Attorney billing number: **5214**

Confirmation number:



**MESSAGE:**

**Patent Application No.: 10/601,136; Our Ref. 81751.0062**
I hereby certify that the following documents:

- **Renewed Petition Under 37 CFR 1.181 (Cover Sheet)**
- **Request for Reconsideration of Petition Pursuant to 37 C.F.R. § 1.181 to Withdraw Holding of Abandonment**
- **Copy of Decision on Petition**
- **Copy of Amendment filed March 10, 2006**
- **Statement Under 37 CFR 1.8(b)(3)**

December 8, 2006
Date of Deposit

Diane Zynn

are being facsimiled to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450., for filing in the above-identified application.

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DEC 08 2006

Appl. No. 10/601,136 Attorney Docket No. 81751.0062
Customer No.: 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Makoto Kudo
Serial No: 10/601,136
Confirmation No.: 5957
Filed: June 20, 2003
For: DATA PROCESSING DEVICE AND ELECTRONIC EQUIPMENT

Art Unit: 2181
Examiner: Vincent Lai

I hereby certify that this correspondence is being transmitted via facsimile to (571) 273-8300:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 on
12-8 06
Date of Deposit
Diane Zynn
Name
Signature 12/8/06 Date

**RENEWED PETITION UNDER 37 CFR 1.181 (COVER SHEET)**

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed are the following documents:

- **Request for Reconsideration of Petition Pursuant to 37 C.F.R. § 1.181 to Withdraw Holding of Abandonment**
- **Copy of Decision on Petition**
- **Copy of Amendment filed March 10, 2006**
- **Statement Under 37 CFR 1.8(b)(3)**

If it should be determined that for any reason either an insufficient fee or an excessive fee has been paid, please charge any insufficiency or credit any overpayment necessary to ensure revival of the above-identified application to Deposit Account No. 50-1314. A copy of this petition is enclosed.

Respectfully submitted,
HOGAN & HARTSON L.I..P.

Date: December 8, 2006

By
Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

1999 Avenue of the Stars, Suite 1400
Los Angeles, California 90067
Phone: 310-785-4600
Fax: 310-785-4601

Appl. No. 10/601,136

Attorney Docket No. 81751.0062
Customer No.: 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Makoto Kudo
Serial No: 10/601,136
Confirmation No.: 5957
Filed: June 20, 2003
For: DATA PROCESSING DEVICE AND ELECTRONIC EQUIPMENT

Art Unit: 2181
Examiner: Vincent Lai

I hereby certify that this correspondence is being transmitted via facsimile to (571) 273-8300:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 on
12-8-06
Date of Deposit
Diane Zynn
Name
Diane Zynn 12/8/06
Signature Date

**REQUEST FOR RECONSIDERATION OF PETITION PURSUANT TO 37 C.F.R. § 1.181 TO WITHDRAW HOLDING OF ABANDONMENT**

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 C.F.R. § 1.181, applicant respectfully petitions to withdraw holding of abandonment of the above-identified patent application which became abandoned on August 4, 2006. The present application became abandoned because the Patent Office informed Troy Schmelzer that a response to the non-final office action mailed out on December 14, 2005 had not been timely received. The attorney contends that a response was sent out on March 10, 2006. Copy of the sent response is enclosed.

In addition, a statement under 37 CFR 1.8(b)(3), by the person who signed the certificate of mailing is attached.

Based on the foregoing, Applicant respectfully requests that the Office Withdraw the Holding of Abandonment of this application.

Applicant believes that no fee is due in connection with the instant petition. However, if it should be determined that for any reason either an insufficient fee or an excessive has been paid, please charge any insufficiency or credit any

Appl. No. 10/601,136

Attorney Docket No. 81751.0062
Customer No.: 26021

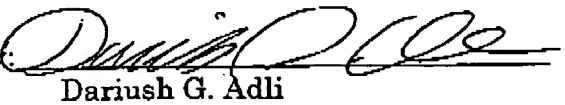
It is believed that no extension of time is required. However, should an extension of time be necessary to revive the above-identified application or to prevent the above-identified application from becoming abandoned again, please consider this a conditional petition for such an extension of time. Please charge any fee for such an extension of time to Deposit Account No. 50-1314. A copy of this paper is enclosed.

If it should be determined that for any reason either an insufficient fee or an excessive fee has been paid, please charge any insufficiency or credit any overpayment necessary to ensure revival of the above-identified application to Deposit Account No. 50-1314. A copy of this petition is enclosed.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: December 8, 2006

By: 
Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

1999 Avenue of the Stars, Suite 1400
Los Angeles, California 90067
Phone: 310-785-4600
Fax: 310-785-4601

Enclosures: Copy of Decision on Petition
Copy of Amendment filed March 10, 2006
Statement under 37 CFR 1.8(b)(3)

UNITED STATES PATENT AND TRADEMARK OFFICE

Sonia Edson / DA

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS SUITE 1400
LOS ANGELES CA 90067

COPY MAILED
OCT 24 2006
OFFICE OF PETITIONS

In re Application of
Makoto Kudo
Application No. 10/601,136
Filed: June 20, 2003
Attorney Docket No. 81751.0062

DECISION ON PETITION

THIS MATTER DOCKETED
FOR 12-26-06 (Req for Reconsideration da

This is decision on the petition filed August 14, 2006, which is being treated as a petition under 37 CFR 1.181 to withdraw the holding of abandonment.

On December 14, 2005, the Office mailed a nonfinal Office action, which set a three-month shortened statutory period for reply. In the apparent absence of a timely filed response, the application became abandoned on March 15, 2006. On August 4, 2006, the Office mailed a Notice of Abandonment.

In the present petition, petitioner asserted that he filed a timely response to the nonfinal Office action on March 10, 2006. In support of the assertion, petitioner submitted a copy of the reply in the form of an amendment, bearing a certificate of mailing dated March 10, 2006. Nevertheless, the record does not show that the USPTO received the amendment. Therefore, petitioner is relying on the certificate of mailing as evidence of the timely filing of the amendment on March 10, 2006.

Pursuant to Section 711.03(c)(I)(B) of the Manual of Patent Examining Procedure:

> Where a certificate of mailing under 37 CFR 1.8, but not a postcard receipt, is relied upon in a petition to withdraw the holding of abandonment, see 37 CFR 1.8(b) and MPEP § 512. As stated in 37 CFR 1.8(b)(3) the statement that attests to the previous timely mailing or transmission of the correspondence must be on a personal knowledge basis, or to the satisfaction of the Director of the USPTO. **If the statement attesting to the previous timely mailing is not made by the person who signed the Certificate of Mailing (i.e., there is no personal knowledge basis), then the statement attesting to the previous timely mailing should include evidence that supports the conclusion that the correspondence was actually mailed (e.g., copies of a mailing log establishing that correspondence was mailed for that application).**

(Emphasis added).

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OCT 26 2006
DOCKETING

Petitioner did not provide a statement under 37 CFR 1.8(b)(3), attesting to a personal knowledge of the mailing of the original response on the date indicated on the certificate **by the person who signed the certificate.**

Accordingly, the petition to withdraw the holding of abandonment is **dismissed**. Before the Office can withdraw the holding of abandonment, petitioner must submit a request for reconsideration and a statement in compliance with 37 CFR 1.8(b)(3). A request for reconsideration of this decision must be submitted with TWO (2) MONTHS of the mailing date of this decision. Extensions of this time period may be granted under 37 CFR 1.136. The request for reconsideration should include a cover sheet entitled "Renewed Petition Under 37 CFR 1.181."

Further correspondence with respect to this matter should be addressed as follows:

By mail: Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX: (571) 273-8300
Attn: Office of Petitions

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Telephone inquiries related to this decision should be directed to the undersigned at (571) 272-3211.

C. T. Donnell

Christina Tartera Donnell
Senior Petitions Attorney
Office of Petitions

Appl. No. 10/601,136

Attorney Docket No. 81751.0062
Customer No.: 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Makoto Kudo
Serial No: 10/601,136
Confirmation No.: 5957
Filed: June 20, 2003
For: DATA PROCESSING DEVICE AND ELECTRONIC EQUIPMENT

Art Unit: 2181
Examiner: Vincent Lai

**STATEMENT UNDER 37 CFR 1.8(b)3**

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

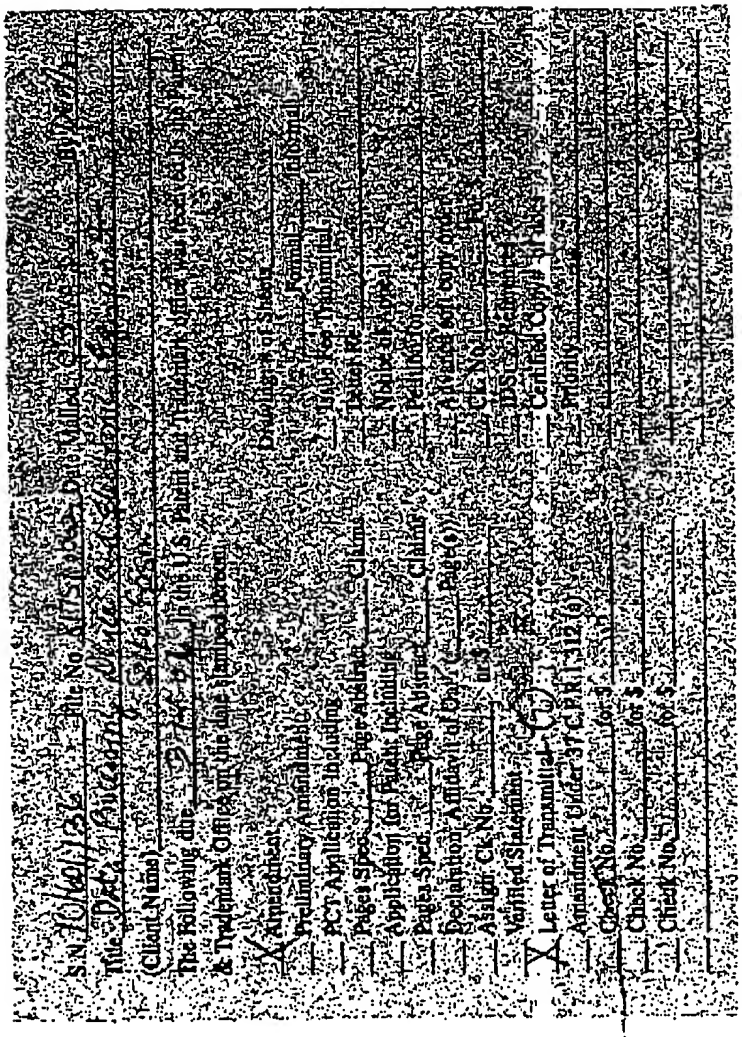
I, Sherlin Yaghoubzadeh, declare that I signed the certificate of mailing dated March 10, 2006.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signed this 4th day of December 2006, at Los Angeles California.

Sherlin Yaghoubzadeh

\\\LA - 081751/000062 - 330811 v1



FORM PTO-1083

81751.0062

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Makoto Kudo
Serial No: 10/601,136
Confirmation No.: 5957
Filed: June 20, 2003
For: DATA PROCESSING DEVICE AND ELECTRONIC EQUIPMENT

Art Unit: 2181
Examiner: Vincent Lai

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450, on
March 10, 2006
Date of Deposit
Sherlin Yaghoubzadeh
Name
Signature
03-10-06
Date

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an amendment in the above-identified application.
☒ No additional fee is required.

The fee has been calculated as shown below:

| | (Col. 1) CLAIMS REMAINING AFTER AMENDMENT | | (Col. 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | | (Col. 3) PRESENT EXTRA* | LG/SM $ ENTITY FEE | | ADD'L FEE DUE |
|---|---|---|---|---|---|---|---|---|
| TOTAL CLAIMS FEE | 20 | - | 20 | ** | 0 | LG=$50 SM=$25 | $[FEE] | $ 0 |
| INDEPENDENT CLAIMS FEE | 2 | - | 3 | *** | 0 | LG=$200 SM=$100 | $[FEE] | $ 0 |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIMS | | | | | | LARGE ENTITY FEE = $360 SMALL ENTITY FEE = $180 | | $ [FEE] |
| ADDITIONAL SIZE FEE (IF ANY) (TOTAL PAGES OF SPEC AND DRAWINGS TOGETHER) | | | | | $250 FOR EACH ADDITIONAL 50 SHEETS | | | $ [FEE] |
| | | | | | | | TOTAL | $ 0 |

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box on Col. 1 of a prior amendment or the number of claims originally filed.

☐ A check in the amount of $ 0 to cover the additional claims fee is enclosed. **A copy of this sheet is enclosed.**

☐ A check in the amount of $ 0 to cover the extension fee is enclosed. **A copy of this sheet is enclosed.**

☒ The Commissioner is hereby authorized to charge any deficiencies of fees associated with this communication or credit any overpayment to Deposit Account No. 50-1314. **A copy of this sheet is enclosed.**
- ☒ Any filing fees under 37 C.F.R. § 1.16 for the presentation of extra claims
- ☒ Any patent application processing fees under 37 C.F.R. § 1.17

Respectfully submitted,
HOGAN & HARTSON L.L.P.

By: _____
Daniush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

Date: March 10, 2006

Biltmore Tower
500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Telephone: 213 337-6700
Facsimile: 213 337-6701

Appl. No. 10/601,136
Amdt. Dated March 10, 2006
Reply to Office Action of December 14, 2005

Attorney Docket No. 81751.0062
Customer No.: 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Makoto Kudo
Serial No: 10/601,136
Confirmation No.: 5957
Filed: June 20, 2003
For: DATA PROCESSING DEVICE AND ELECTRONIC EQUIPMENT

Art Unit: 2181
Examiner: Vincent Lai

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
March 10, 2006
Date of Deposit
Sherlin Yashoubzadeh
Name
Signature
03-10-06
Date

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated December 14, 2005, please amend the above-referenced application as follows:

**Amendments** to the specification begin on page 2 of this paper.

**Amendments** to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

**Remarks/Arguments** begin on page 12 of this paper.

**Amendments to the Specification:**

Please replace the Title with the following rewritten Title:

DATA PROCESSING DEVICE AND ELECTRONIC EQUIPMENT FOR PERFORMING PIPELINE CONTROL

Please replace the Abstract with the following rewritten Abstract:

~~A high cost performance data processing device and electronic equipment are capable of executing an instruction set including a prefix instruction without increasing the circuit scale.~~ The data processing device and electronic equipment of the present invention perform ~~performs~~ pipeline control and include ~~includes~~ a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues. ; A ~~a~~ prefix instruction decoder circuit ~~which~~ performs a decode processing only on a prefix instruction. ; The ~~the~~ prefix instruction decoder circuit receives ~~receiving~~ the instruction code before decoding, judges ~~judging~~ whether or not the instruction is a given prefix instruction, and causes ~~causing~~ a target instruction to modify an ~~modifying~~ information register to store information necessary for decoding a target instruction when the instruction is the given prefix instruction. ; A ~~and a~~ decoder circuit ~~which~~ receives each of the instruction codes of the instructions other than the prefix instruction as a decode instruction and decodes the decode instruction. When the decode instruction is a target instruction, the target instruction modified by the prefix instruction is decoded based on the target instruction modifying information.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A data processing device which performs pipeline control, the data processing device comprising:

a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues, the instructions including a given target instruction and a prefix instruction which precedes the target instruction and modifies a function of the target instruction;

a prefix instruction decoder circuit which performs decode processing only on a prefix instruction, the prefix instruction decoder circuit receiving the instruction codes of the instructions before decoding that are fetched in the instruction queues, judging whether or not each of the instruction codes is a given prefix instruction, and causing a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction; and

a general-purpose decoder circuit which receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction, and decodes the decode instruction,

wherein, when the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register.

wherein the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction.

2. (Original) The data processing device as defined in claim 1,

wherein the given prefix instruction includes an immediate-data expansion prefix instruction for expanding immediate data necessary for execution of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store immediate-data expansion information necessary for expanding the immediate data during execution of the target instruction modified by the immediate-data expansion prefix instruction when the input instruction code is the immediate-data expansion prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the immediate data is expanded at the time of execution of the target instruction that has been modified by the immediate-data expansion prefix instruction based on the immediate-data expansion information stored in the target instruction modifying

information register when the decode instruction is the target instruction of the immediate-data expansion prefix instruction.

3. (Cancelled).

4. (Original) The data processing device as defined in claim 1,

wherein the given prefix instruction includes a register expansion prefix instruction for expanding a register necessary for execution of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store register expansion information necessary for expanding the register during execution of the target instruction modified by the register expansion prefix instruction when the input instruction code is the register expansion prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the register is expanded at a time of execution of the target instruction that has been modified by the register expansion prefix instruction based on the register expansion information stored in the target instruction modifying information register when the decode instruction is the target instruction of the register expansion prefix instruction.

5. (Currently Amended) A ~~The~~ data processing device ~~as defined in claim 1,~~ which performs pipeline control, the data processing device comprising:

a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues, the instructions including a given target instruction and a prefix instruction which precedes the target instruction and modifies a function of the target instruction;

a prefix instruction decoder circuit which performs decode processing only on a prefix instruction, the prefix instruction decoder circuit receiving the instruction codes of the instructions before decoding that are fetched in the instruction queues, judging whether or not each of the instruction codes is a given prefix instruction, and causing a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction; and

a general-purpose decoder circuit which receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction, and decodes the decode instruction,

wherein, when the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register,

wherein the given prefix instruction includes an execution control prefix instruction for controlling whether or not to execute the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store execution control information necessary for controlling whether or not to execute the target instruction modified by the execution control prefix instruction when the input instruction code is the execution control prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the target instruction modified by the execution control prefix instruction is executed by judging whether or not to execute the target instruction based on the execution control information stored in the target instruction modifying information register

when the decode instruction is the target instruction of the execution control prefix instruction.

6. (Original) The data processing device as defined in claim 1,

wherein the fetch circuit is connected with a bus having a width at least twice the width of the instruction code, and fetches the instructions in the instruction queues through the bus in one clock cycle.

7. (Original) The data processing device as defined in claim 1,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

8. (Currently Amended) The data processing device as defined in claim 5 ~~2~~,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

9. (Original) The data processing device as defined in claim 3,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first

instruction during a period in which the decoder circuit decodes the first instruction.

10. (Original) The data processing device as defined in claim 4,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

11. (Original) The data processing device as defined in claim 5,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

12. (Original) The data processing device as defined in claim 6,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

13. (Original) Electronic equipment comprising:

the data processing device as defined in claim 1;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

14. (Currently Amended) Electronic equipment comprising:

the data processing device as defined in claim 5 ~~2~~;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

15. (Cancelled).

16. (Original) Electronic equipment comprising:

the data processing device as defined in claim 4;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

17. (Original) Electronic equipment comprising:

the data processing device as defined in claim 5;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

18. (Original) Electronic equipment comprising:

the data processing device as defined in claim 6;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

19. (Original) Electronic equipment comprising:

the data processing device as defined in claim 7;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

20. (New) The data processing device as defined in claim 5,

wherein the given prefix instruction includes an immediate-data expansion prefix instruction for expanding immediate data necessary for execution of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store immediate-data expansion information necessary for expanding the immediate data during execution of the target instruction modified by the immediate-data expansion prefix instruction when the input instruction code is the immediate-data expansion prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the immediate data is expanded at the time of execution of the target instruction that has been modified by the immediate-data expansion prefix instruction based on the immediate-data expansion information stored in the target instruction modifying information register when the decode instruction is the target instruction of the immediate-data expansion prefix instruction.

21. (New) The data processing device as defined in claim 5,

wherein the given prefix instruction includes a register expansion prefix instruction for expanding a register necessary for execution of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store register expansion information necessary for

expanding the register during execution of the target instruction modified by the register expansion prefix instruction when the input instruction code is the register expansion prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the register is expanded at a time of execution of the target instruction that has been modified by the register expansion prefix instruction based on the register expansion information stored in the target instruction modifying information register when the decode instruction is the target instruction of the register expansion prefix instruction.

22. (New) The data processing device as defined in claim 5,

wherein the fetch circuit is connected with a bus having a width at least twice the width of the instruction code, and fetches the instructions in the instruction queues through the bus in one clock cycle.

## REMARKS

This application has been carefully reviewed in light of the Office Action dated December 14, 2005. Claims 1-22 remain in this application. Claims 1 and 5 are the independent claims. Claims 1, 5, 8 and 14 have been amended. Claims 3 and 15 have been cancelled, without prejudice. Claims 20-22 have been added. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

### Specification Objections

The abstract was objected to for undue length. In response, the abstract has been amended to comply with MPEP §608.01(b). Reconsideration of the abstract, as amended, is respectfully requested.

The title was objected to for being non-descriptive. In response, the title has been amended to more distinctly describe the invention. Reconsideration of the title, as amended, is respectfully requested.

### Art-Based Rejections

Claims 1-2, 5-8, 11-14 and 17-19 were rejected under 35 U.S.C. §102(b) over US 5,822,559 (Narayan); Claims 3, 9 and 15 were rejected under 35 U.S.C. §103(a) over Narayan in view of US 6,260,134 B1 (Zuraski); and Claims 4, 10 and 16 were rejected under 35 U.S.C. §103(a) over Narayan in view of US 2002-0056035 A1 (Rozenshein).

Applicant respectfully traverses these rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

**The Narayan Reference**

Narayan discloses a microprocessor having a plurality of early decode units configured to detect double dispatch instructions and to dispatch these instructions to a pair of decode units. Complex instructions are executed serially by an MROM unit, and simple instructions are dispatched to a single decode unit. *(See Narayan, Col. 3, lines 7-14).*

**The Zuraski Reference**

Zuraski is directed to a predecode unit configured to predecode a fixed number of instruction bytes of variable length instructions per clock cycle. The predecode unit outputs predecode bits which identify whether any of the predecoded instruction bytes are the start byte of an instruction. An instruction alignment unit then uses the start bits to dispatch the variable byte-length instructions to a plurality of decode units that form fixed issue positions within a processor. *(See Zuraski; Col. 2, line 60 to Col. 3, line1).*

**The Rozenshein Reference**

Rozenshein is directed to an instruction system that includes an instruction root having an operation selection field for selecting an operation to be performed by a data processor and an instruction prefix. *(See Rozenshein; Par. [0024]).*

**The Claims are Patentable Over the Cited References**

The present application is generally directed to a data processing device that performs pipeline control.

As defined by independent Claim 1, a data processing device which performs pipeline control includes a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues. The instructions include a given target

instruction and a prefix instruction which precedes the target instruction and modifies a function of the target instruction. A prefix instruction decoder circuit performs decode processing only on a prefix instruction. The prefix instruction decoder circuit receives the instruction codes of the instructions before decoding that are fetched in the instruction queues, judges whether or not each of the instruction codes is a given prefix instruction, and causes a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction. A general-purpose decoder circuit receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction and decodes the decode instruction. When the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register. The given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction. The prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction. The decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "wherein the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction," as required by amended independent Claim 1. In addition, the applied references do not disclose or suggest, "wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction," as required by amended independent Claim 1. Moreover, the applied references do not disclose or suggest, "wherein the decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction," as required by amended independent Claim 1.

The Office Action concedes that Narayan does not disclose that the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction.

The Office Action purports that Zuraski discloses the use of a prefix instruction that is predecoded (or decoded before the main decoder) in order to simplify circuitry. *(See Zuraski; Col. 13, line 65 to Col. 14, line 1).*

However, Zuraski discloses that, because the instruction length is variable, the multiplexer must be able to shift the instruction bytes suitably (in order to adjust a variety of instruction lengths), which increases the complexity of the

multiplexer. By predecoding a fixed number of instruction bytes, the multiplexer processes the instruction bytes. *(See Zuraski; Col. 2, lines 49-57; Col. 3, lines 1-5)*. Thus, Zuraski fails to disclose the features of amended Claim 1. Even though Zuraski discloses shifting an instruction code, Zuraski fails to shift an execution result of a target instruction, as recited in the claims of the present invention. Moreover, Zuraski discloses shifting the positions of instruction bytes for adjustment, but fails to disclose storing shift information necessary for shifting execution results of the target information in the target instruction modifying information register nor shifting the information stored in the target instruction modifying information register, as recited in the claims of the present invention.

In contrast to Narayan and Zuraski, the claims of the present invention require that the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction. The prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction. The decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction. Accordingly, the present invention performs predetermined pipeline control for operation processing in which execution results of a target instruction are shifted arithmetically or logically and, thus, has an objective which is different from those of the cited references.

Narayan and Zuraski, alone or in combination, do not disclose or suggest these features of the present invention as required by amended Claim 1, and Rozenshein does not remedy the deficiencies of Narayan and Zuraski.

Since the applied references do not disclose or suggest the above features of the present invention as required by amended independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claim 1, as amended, is believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that amended independent Claim 5 is allowable for at least the same reasons as discussed above in reference to amended independent Claim 1 and such allowance is respectfully requested.

The remaining claims depend either directly or indirectly from amended independent Claims 1 and 5 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are also believed to be in condition for allowance and such allowance is respectfully requested.

## Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: March 10, 2006

By: 

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